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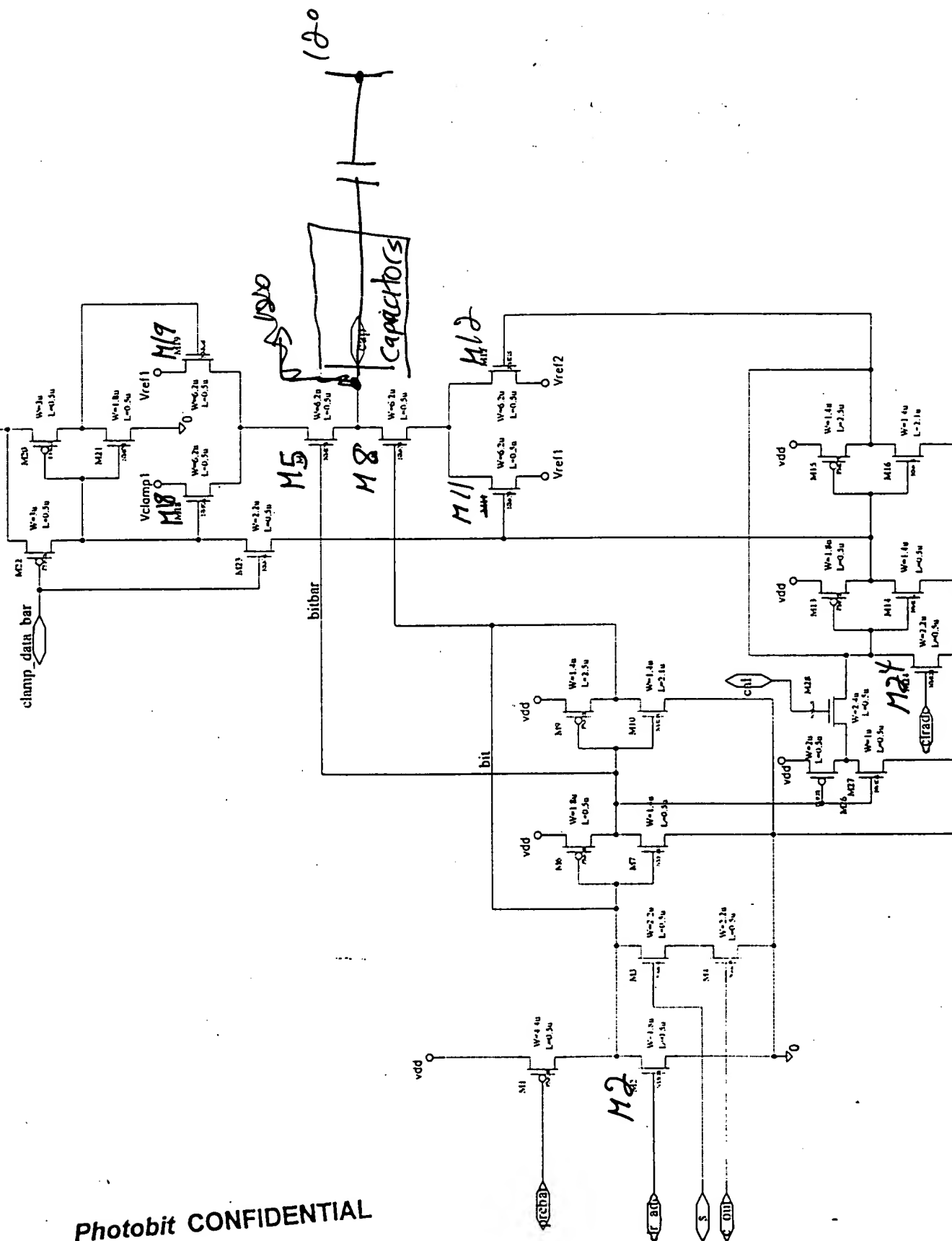


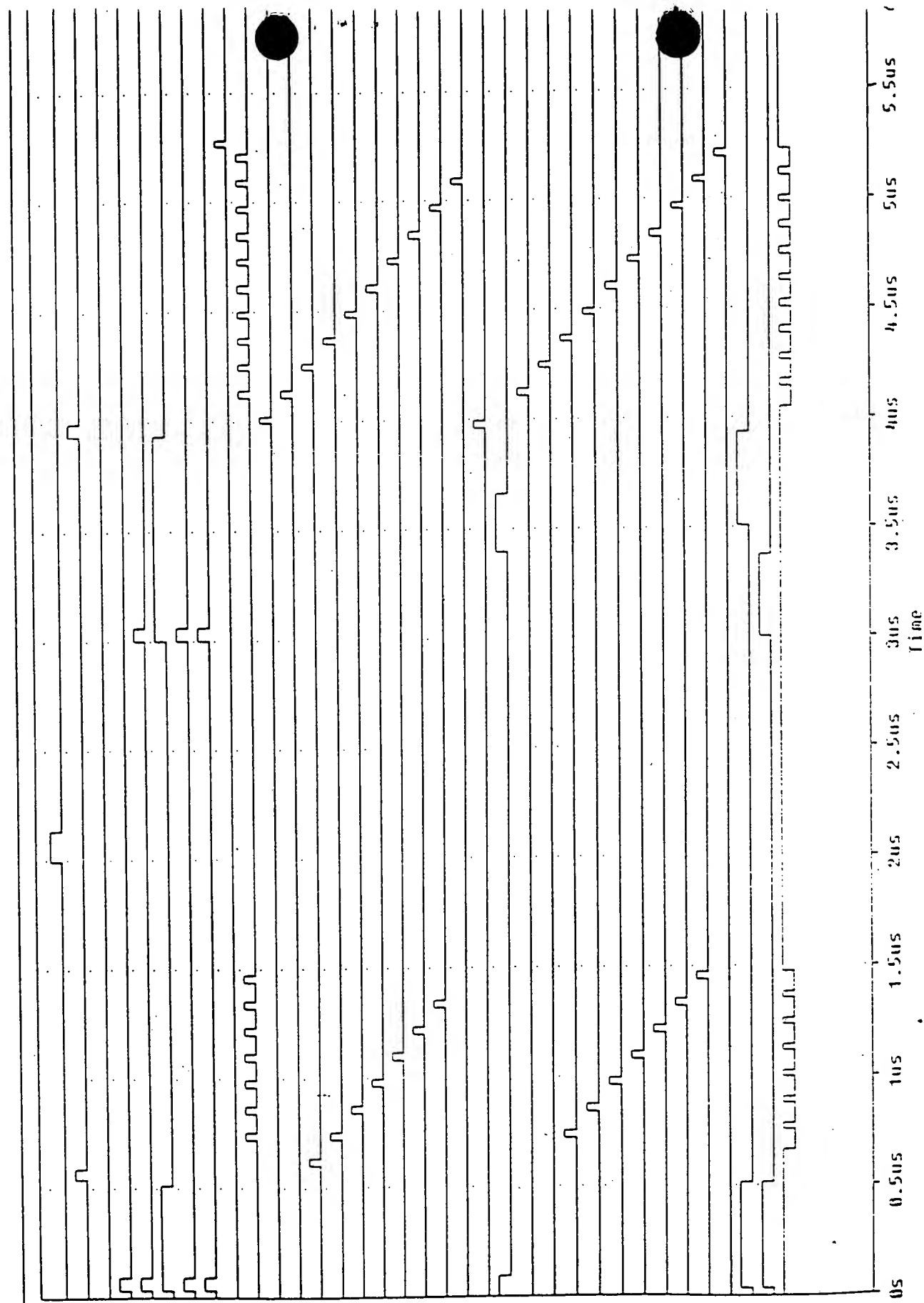
Fig. 2

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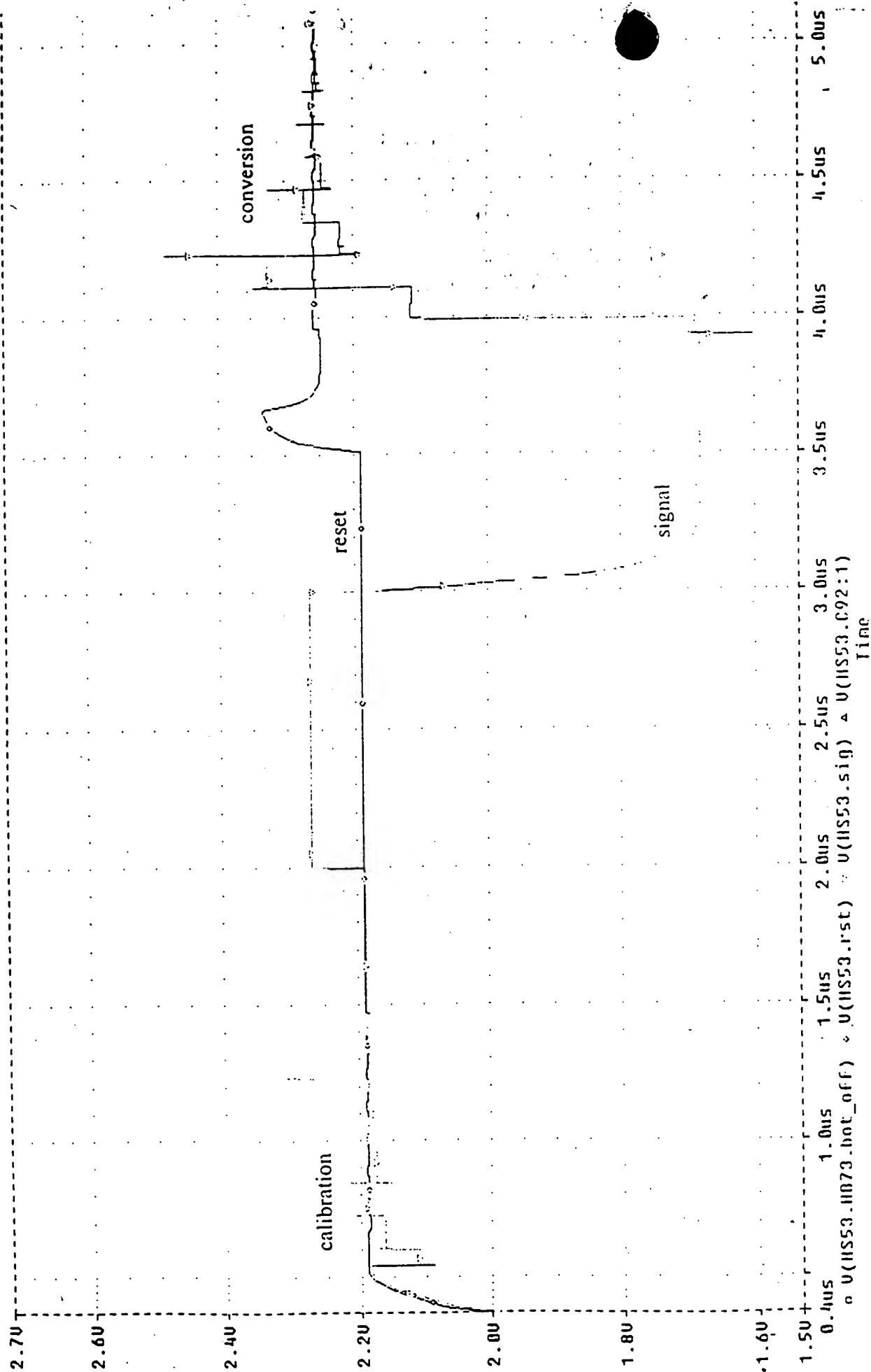
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pre_3
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pre_8
pre_9
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rst_en
s_0
s_1
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s_6
s_7
s_8
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shr
shs
Stroke#

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3.

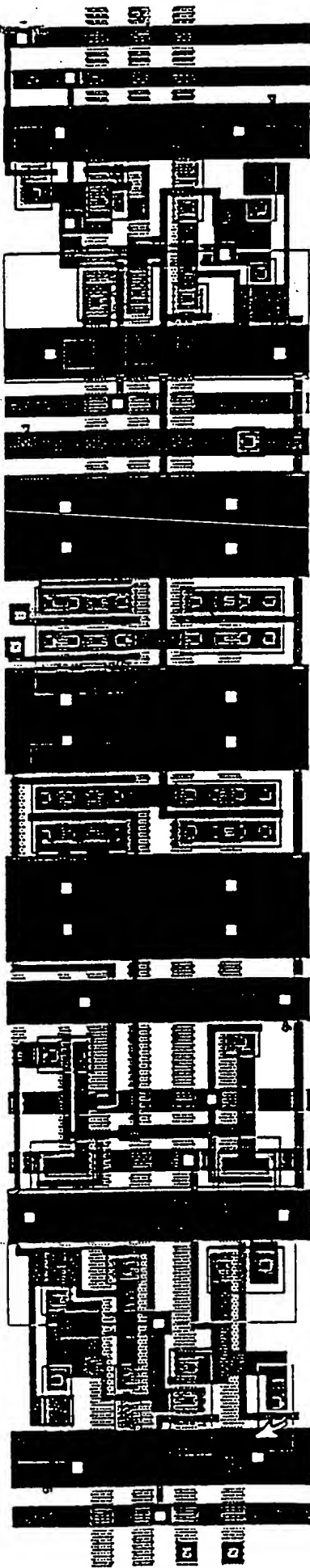
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Fig. 4

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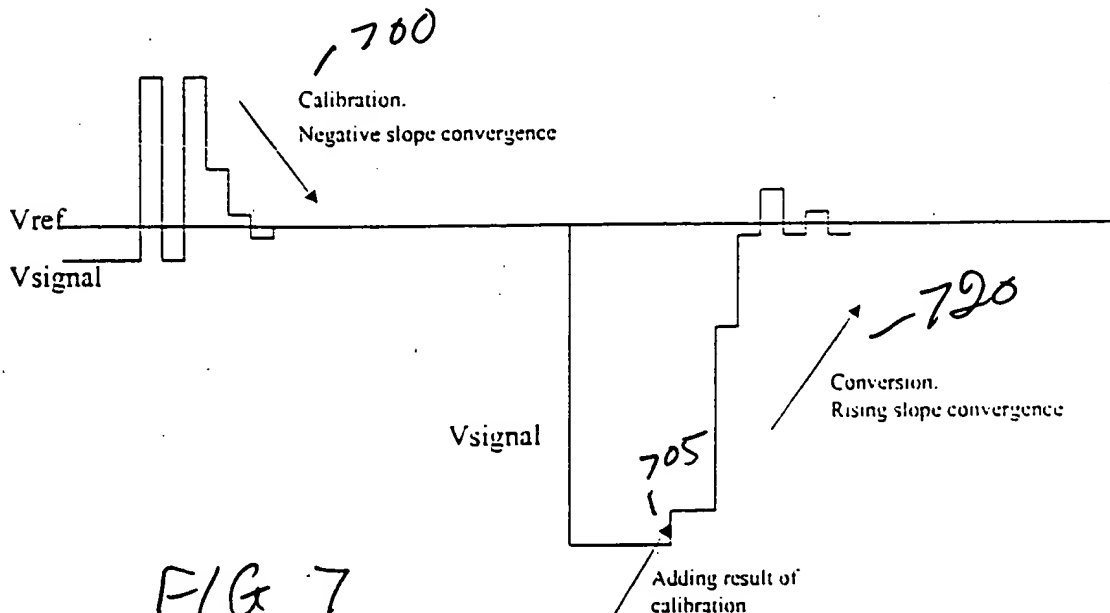
Fig 5



## METHOD2.

The drawbacks of the method 1 is the need to calculate the negative value in latches. Although, the negative can be substituted with the two's complement, the error because of the substitution is 1 LSB. For better accuracy one needs either a real adder in latches, or one extra calibration smallest bit.

The method proposed here is based on a negative slope convergence during the calibration, followed by positive slope approximation during the conversion. The sketch of what the convergence process will look like is presented below



The ADC circuitry and example of the operation are presented in the following drawings. Note, that both comparator outputs, negative and positive are used for operation.

Sequence of operations (calibration, conversion) is the following:

- Signal for calibration is sampled while bottom plates of calibration capacitors seat at  $V_{ref}$ . This will allow adding some negative compensation signal during calibration. But, prior to start calibration, a positive offset is added through capacitor C offset.
- During calibration, a negative compensation code is determined and stored in latches.
- To start conversion, the calibration value must be added to the signal. This is done in two steps:
  - a) for those latches which keep "0" bottom plates during signal sampling must seat at ground
  - b) for latches with "1" they must seat at  $V_{ref}$ .

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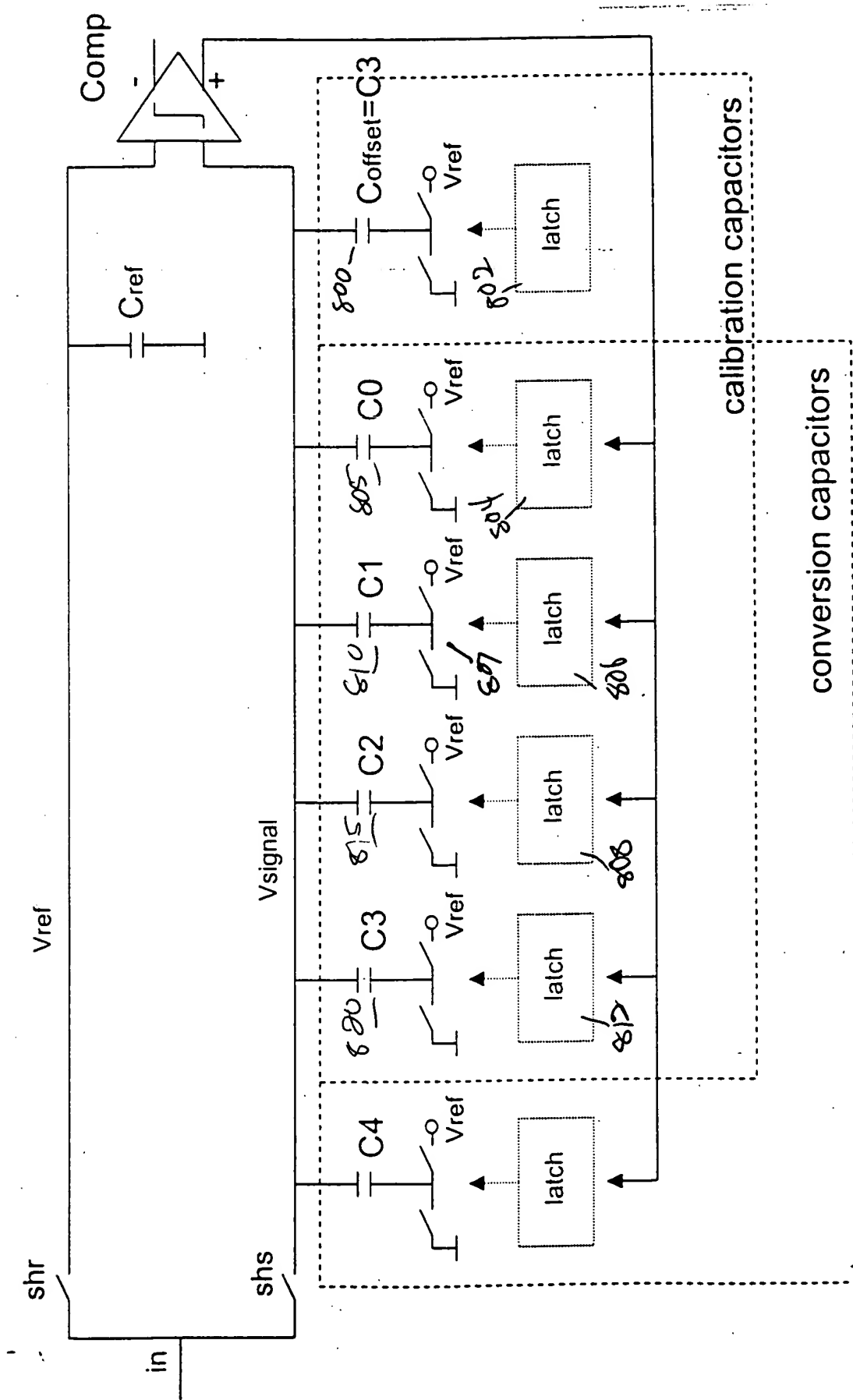


Fig 8